**Project 6 Evaluation**

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| Name: | | Total: | |
| Checklist | Weight | Earned | Notes |
| 1. Description of design approach | 10 |  |  |
| 1. Model Composer integration of QR Decomposition and matrix-vector multiplication  * Block diagrams * Scope/ terminal text outputs * Alternate version if QRD and matrix-vector done in Vitis HLS | 20 |  |  |
| 1. Integration with ARM core on the Zynq ZedBoard  * Block diagram * Back-substitution and test bench C++ code (Vitis C++ code to start QRD, matric vector multiplication on PL, then C++ back substitution on PS ARM core.) * Terminal text outputs | 20 |  |  |
| 1. Stand-alone C++ code version of the entire linear equation solver algorithm (with QR Decomposition)  * C++ Code * Terminal text outputs * Timing results | 20 |  |  |
| 1. Timing analysis of the design tradeoffs between the totally stand-alone C++ version and the FPGA SoC PL accelerated version. | 10 |  |  |
| 1. Demonstration of the array being able to solve three different instances of systems of equations for both the stand-alone C++ versions and also the FPGA SoC PL accelerated version.  * Documentation of the timings for each system of equations, and the total time for all three for both the stand-alone C++ versions and also the FPGA SoC PL accelerated version | 10 |  |  |
| 1. Turning in the required files | 10 |  |  |
| 1. Extra credit options (10 points each): Matrix-Vector on FPGA, Pipeline multiple matrices, complex data, or GPU | 10-40 |  |  |